

<b>Notice of References Cited</b>		Application/Control No. 09/965,521	Applicant(s)/Patent Under Reexamination ARCHAMBAULT, ROCH GEORGE	
		Examiner Satish S. Rampuria	Art Unit 2124	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
A	US-2002/0166115 A1	11-2002	SASTRY, A.V.S.	717/151
B	US-6,182,284 B1	01-2001	Sreedhar et al.	717/146
C	US-6,487,716 B1	11-2002	Choi et al.	717/159
D	US-5,850,549 A	12-1998	Blainey et al.	717/156
E	US-5,812,855 A	09-1998	Hiranandani et al.	717/157
F	US-5,555,417 A	09-1996	Odnert et al.	717/159
G	US-5,175,856 A	12-1992	Van Dyke et al.	717/151
H	US-5,878,261 A	03-1999	Holler et al.	717/157
I	US-			
J	US-			
K	US-			
L	US-			
M	US-			

**FOREIGN PATENT DOCUMENTS**

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
N					
O					
P					
Q					
R					
S					
T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
U		Kandemir et al., A framework for interprocedural locality optimization using both loop and data layout transformations, Sept. 1999, IEEE, Pages:95 - 102
V		Genin et al., System design, optimization and intelligent code generation for standard digital signal processors, May 1989, IEEE, vol. 1, Pages:565 - 569
W		Carr et al., Compiler optimization for improving data locality, 1994, IEEE, Pages 252-262
X		

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.